IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	GARY M. JOHNSON	Group Art Unit:	2816
Serial No.:	10/733,605	Examiner:	Dinh Thanh Le
Filed:	DECEMBER 11, 2003	Conf. No.:	8519
		Atty. Dkt.:	2008.007900/03-0478
For:	SWITCHED CAPACITOR FOR A TUNABLE DELAY CIRCUIT	CUSTOMER NO.:	23720

REPLY BRIEF

CERTIFICATE OF MAILING
37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below:

December 18, 2007
Date

Signature

MAIL STOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant hereby submits this Reply Brief in response to the Examiner's Answer mailed October 18, 2007. The two-month statutory response date is December 18, 2007. This Reply Brief is being filed on or before the due date, therefore, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

No fee is believed to be due as a result of this filing. However, should any fee(s) under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Commissioner is

authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.087800.

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REMARKS

Appellant respectfully disagrees with Examiner's assertions in the Examiner's Answer. As described in the Appeal Brief, the Examiner cites various prior art references that are directed to passive capacitors. Again, in the Examiner's Answer, the Examiner focuses on capacitors being switched by transistors. The Examiner argues that claims do not call for active capacitors or passive capacitors, but they call for transistive capacitive delay. The Examiner then argues that transistors connected to passive capacitors anticipate or make obvious transitive capacitive delays. However, the Examiner is incorrect in this assumption. The claims, indeed, call for "transistive capacitive delay". Those skilled in the art, upon a reading of the present disclosure, would understand that transistive capacitive delay does not refer to passive capacitors. Again, the Examiner merely points to the disclosure in U.S. Patent No. 5,101,117 (***Johnson***) to argue that the capacitors (72*a-l*) amount to transistive capacitors. ***Johnson*** merely refers to these capacitors (72*a-l*) as "load capacitors." *See* col. 4, lines 62-65. ***Johnson*** specifically labels the devices marked 71*a-l* as "transistors" and the devices marked 72*a-l* as "capacitors." *See* col. 4, lines 39-55. ***Johnson*** does not recite that the capacitors 72*a-l* are transistive capacitors. *Id.* As explained in greater detail in the Appeal Brief, these capacitors are not described as being transistive-type capacitors; they're merely referred to as load capacitors. *See* col. 4, lines 39-55; col. 4, lines 62-65. As described in the Appeal Brief, the cited prior art do not refer to the transitive capacitive delay, as called for by claims of the present invention.

Further, the Examiner asserts that U.S. Patent No. 6,445,231 (***Baker***), in view of U.S. Patent No. 6,483,359 (***Lee***) and in further view of ***Johnson***, do indeed, disclose the

transistive capacitive delay without further arguments, other than to indicate that the Appellants' arguments are not persuasive. As described in detail in the Appeal Brief, the deficit of ***Johnson*** is not made up for by ***Baker*** or ***Lee***. ***Baker*** clearly does not disclose a DLL circuit; however, the Examiner asserts that the modified delay locked loop of ***Baker*** would provide the delay circuit with the transitive capacitive delay of claims of the present invention. This is simply not the case. ***Baker*** does not disclose a DLL circuit comprising a delay circuit, and as described in the Appeal Brief, none of the cited prior art makes obvious activating a transistive capacitive delay, as employed by the present invention.

In the Examiner's Answer, the comments regarding the light bulb, the point made by the Appellants was that the Examiner's argument that attaching a transistor or a switching element to a passive capacitor being able to make obvious the switching of the transitive capacitive delay of claims would be tantamount to arguing that switching any object using a transistor qualifies as a transistive version of that object. For example, using the Examiner's reasoning, a light bulb connected to a transistor switch would fall under the Examiner's category of being transistive, which of course, is incorrect. This analogy was provided by Appellant to illustrate the over-broadness of the Examiner's arguments by stretching the logic of equating a transistive switch attached to a capacitor to make obvious a switching of a transitive capacitive delay, as called for by claims of the present invention. Contrary to the Examiner's arguments, the load capacitors 72a-72l of ***Johnson*** are not transistive capacitive delays, but are simply capacitors that are attached to transistors that behave as switches. This is in contrast to the transistive capacitor delay as called for by claim 1 in the context of the disclosure of the present application. As

exemplified in Figure 5, the transistors that are being switched themselves provide a transistive delay unlike any of the cited prior art, alone or in combination. Therefore, the combination of the cited prior art do not make obvious all of the elements of claims of the present invention.

Still further, regardless of the lack of transistive capacitive delay of ***Johnson***, it is clear that those skilled in the art would not combine ***Johnson*** and ***Lee*** in the manner suggested by the Examiner that would cause one skilled in the art to make obvious all of the elements of claims of the present invention. The Examiner provides no evidence as to why ***Johnson*** and ***Lee*** would be combined by those skilled in the art in the manner suggested by the Examiner.

Applicant respectfully asserts that ***Johnson***, ***Lee***, ***Baker*** and/or their combination do not teach or disclose all of the elements of claims of the present invention. In order to establish a *prima facie* case of obviousness, the Examiner must consider the following factors: 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings; 2) there must be a reasonable expectation of success; and 3) the prior art reference(s) must teach or suggest all the claim limitations. MPEP § 2143 (2005) (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). In making an obviousness rejection, it is necessary for the Examiner to identify the reason why a person of ordinary skill in the art would have combined the prior art references in the manner set forth in the claims. *KSR Int'l Co. v. Teleflex, Inc.*, at 14, No. 04-1350 (U.S. 2007). Applicants respectfully submit that the Examiner has not met this burden. If fact, as illustrated in the Appeal Brief, ***Johnson***,

Lee, and/or ***Baker*** are incompatible, and consequently those skilled in art would not combine them and make all of the elements of claims of the present invention obvious. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established in rejecting claims of the present invention.

Those skilled in the art would not combine ***Baker*** with ***Lee*** and/or ***Johnson*** to make obvious all of the elements of claims of the present invention. Simply because ***Lee*** and ***Johnson*** disclose a DLL loop, the Examiner failed to provide any evidence motivation why those skilled in the art would combine them to make obvious the elements of claims of the present invention, particularly, the delay circuit for activating a transistive capacitive delay. Nothing in ***Lee*** discloses or suggests that those skilled in the art would look for a solution for the transistive capacitor delay and attempt to combine any prior art cited. There are advantages of providing a relatively constant capacitance during voltage transitions. These are motivations that are not addressed or anticipated by ***Lee*** nor ***Johnson***. Without improper hindsight, those skilled in the art simply would not find the motivation to combine the delay lock loop of ***Lee*** with the data path disclosure of ***Johnson***. The Examiner failed to identify the reason why a person of ordinary skill in the art would have combined ***Baker***, ***Lee*** and/or ***Johnson*** in the manner set forth in the claims. *KSR Int'l Co. v.* at 14. Accordingly, the Examiner failed to show a *prima facie* case of obviousness of the pending claims of the present invention.

Further, as the Examiner stated, claims 5-8, 29-32 and 39-41 contain allowable subject matter; however, in light of the arguments presented herein, all pending claims of the present invention are allowable.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-16 and 26, over the prior art of record. Therefore, Appellant respectfully solicits a Notice of Allowance, allowing claims 1-10 and 25-44 of the present invention.

The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments, or suggestions relating to this appeal.

If for any reason the Examiner finds the application other than in condition for allowance, **the Examiner is requested to call the undersigned attorney** with respect to any questions, comments, or suggestions relating to this appeal, at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
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Date: December 18, 2007

By: _____

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